RECEIVED
CENTRAL FAX CENTER
MAY 2 2 2007

In the Claims:

Please amend claims 1-15 as indicated below. This listing of claims replaces all prior versions.

1. (Currently Amended) A method for writing a data value to a location within non-volatile (NV) memory of a smart card, the smart card having a processor that is adapted to read from and write to the NV memory, the method comprising:

providing an instruction to the processor of the smart card, the instruction containing the data value and an address pointer that identifies the location within the NV memory; and

using the processor, writing the data value to the location within the NV memory identified by the address pointer.

~~A method for writing to NV memories in a controller architecture, characterized in that (a) defined data value(s) or (a) defined data word(s) is/are written to (a) defined destination address(es) within the NV memory, by writing the data value(s) or the data word(s) to the predetermined position of the cache page register of the NV memory and updating the page address pointer registers of the NV memory.~~

2. (Currently Amended) A method as claimed in claim 1, characterized in that, for writing to the NV memory, ~~the~~ an instruction set of the ~~controller core~~ processor is extended by additional move code write instructions (MOVCWR instructions).

3. (Currently Amended) A method as claimed in claim 2 [[1]], characterized in that the additional instructions of the ~~controller core~~ processor perform a transfer of ~~the~~ parameters for the address pointer[[s]] and for the data value to be written ~~or the data word to be written~~ and activate corresponding control signals for a memory management unit (MMU) and NV memory interfaces.

4. (Currently Amended) A method as claimed in claim 2 [[1]], characterized in that ~~the~~ address processing for the MOVCWR instructions is performed in the same way as the

processing of code fetches or MOVC instructions, in the presence of a memory management unit (MMU).

5. (Currently Amended) A method as claimed in claim 3 [[1]], characterized in that ~~this~~ the MMU is extended by a control signal path in the presence of a memory management unit (MMU) of the ~~controller~~ processor.

6. (Previously Presented) A method as claimed in claim 1, characterized in that, in the presence of an MMU, only address areas of the NV memory are written to which have been enabled by the MMU.

7. (Currently Amended) A method as claimed in claim 1, characterized in that special mapping of ~~the~~ code memory is taken into account within ~~the~~ an address area of the processor ~~controller~~ in the presence of an MMU.

8. (Currently Amended) A method as claimed in claim 1, characterized in that a plurality of data values ~~and/or data words~~ with ~~the~~ a same page address are written in succession.

9. (Currently Amended) A method as claimed in claim 1, characterized in that the content of ~~the~~ a cache page register is programmed into the NV memory by writing to ~~the~~ a control register of the NV memory.

10. (Currently Amended) A method as claimed in claim 9 [[1]], characterized in that the cache page register of the NV memory is cleared when changing to a new page address in ~~the~~ an event of an MOVCWR instruction.

11. (Currently Amended) A method as claimed in claim 1, characterized in that undesired programming of old page register contents under incorrect addresses is prevented.

12. (Currently Amended) A smart card comprising:

non-volatile (NV) memory;

an input/output for receiving an instruction, the instruction containing a data value to be written to a location within the NV memory and an addresses pointer that identifies the location; and

a processor that is adapted to write the data value to the location within the NV memory identified by the address pointer in response to the instruction, the processor further adapted to read from the NV memory.

~~An arrangement having a processor, which is designed in such a way that writing to NV memories in a controller architecture may be performed, wherein (a) defined data value(s) or (a) defined data word(s) is/are written to (a) defined destination address(es) within the NV memory, by writing the data value(s) or the data word(s) to the predetermined position of the cache page register of the NV memory and updating the page address pointer registers of the NV memory.~~

13. (Currently Amended) ~~An arrangement having a processor~~ A smart card as claimed in claim 12, characterized in that the processor is ~~part of a smart card controller and the arrangement is a smart card~~ adapted to write the data value to the location within the NV memory by writing the data value to a control register of the NV memory.

14. (Currently Amended) A computer program product which comprises a computer-readable storage medium, on which a program is stored which, once it has been loaded into ~~the~~ memory of a computer or of a smart card processor ~~controller~~, allows the computer or smart card processor ~~controller~~ to perform writing to NV memory[[ies]] in a smart card ~~controller architecture~~, wherein ~~(a) defined~~ a data value~~(s) or (a) defined data word(s)~~ is/~~are~~ written to ~~(a) defined destination address(es)~~ a location within the NV memory that is identified by an address pointer, by writing the data value~~(s) or the data word(s) to the predetermined position of the~~ to a cache page register of the NV memory and updating ~~the~~ page address pointer registers of the NV memory, the data value and the address pointer contained in an instruction.

15. (Currently Amended) A smart card comprising:

non-volatile (NV) memory means;

means for receiving an instruction, the instruction containing a data value to be written to a location within the NV memory and an addresses pointer that identifies the location; and

a processor means that is adapted to write the data value to the location within the NV memory identified by the address pointer in response to the instruction, the processor means further adapted to read from the NV memory.

~~A computer-readable storage medium, on which a program is stored which, once it has been loaded into the memory of a computer or of a smart card controller, allows the computer or smart card controller to perform writing to NV memories in a controller architecture, wherein (a) defined data value(s) or (a) defined data word(s) is/are written to (a) defined destination address(es) within the NV memory, by writing the data value(s) or the data word(s) to the predetermined position of the cache page register of the NV memory and updating the page address pointer registers of the NV memory.~~